02-0001845)

FIG. 1

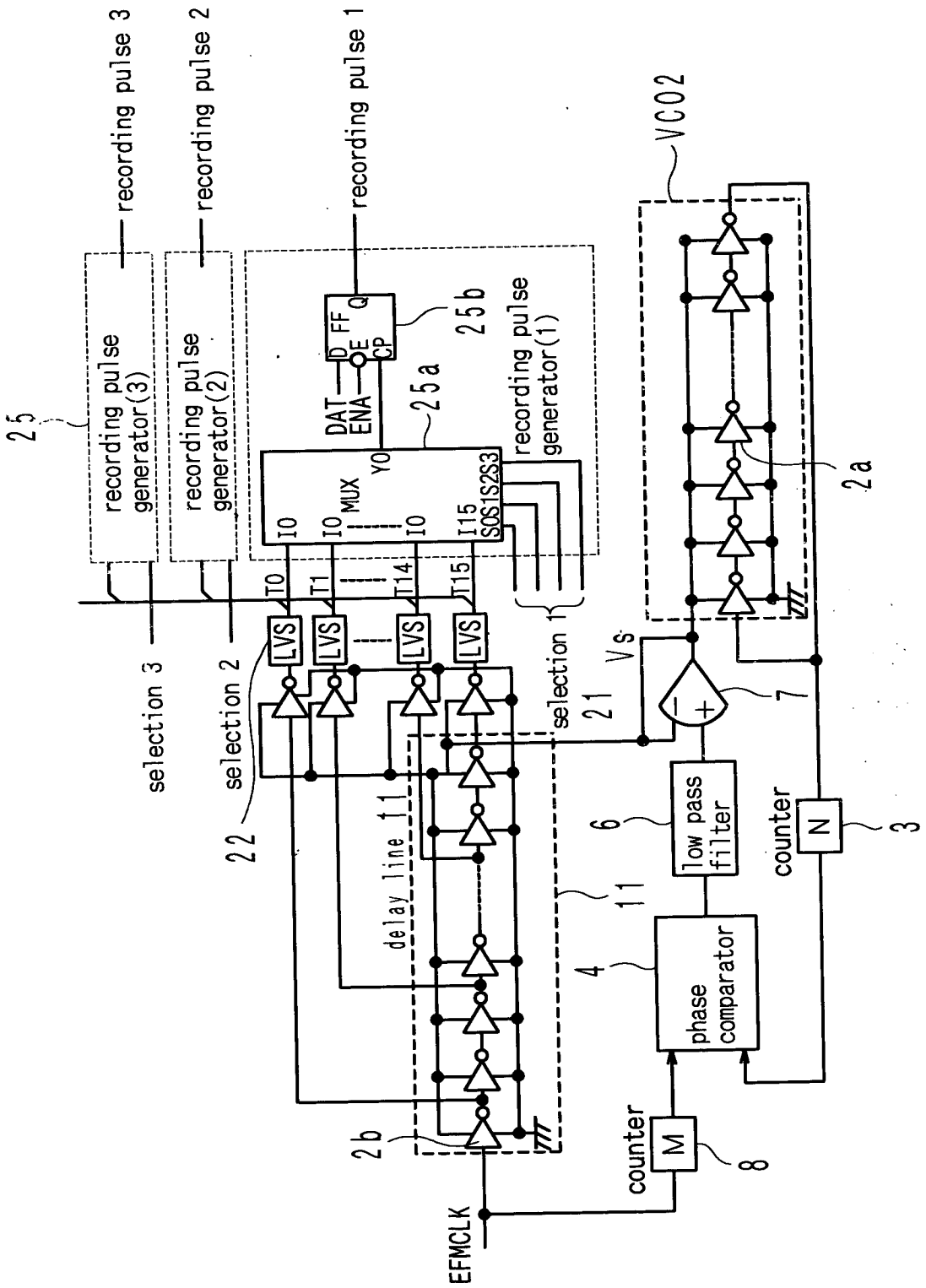


FIG. 2

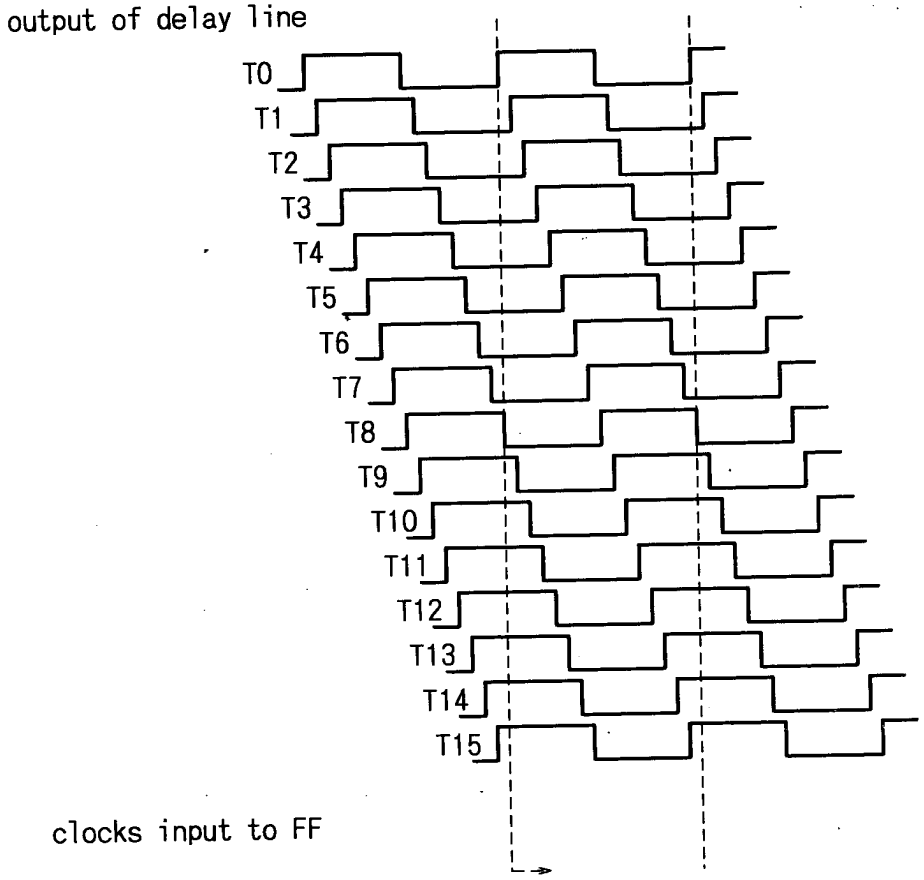

output of delay line
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
T15
clocks input to FF

FIG. 3

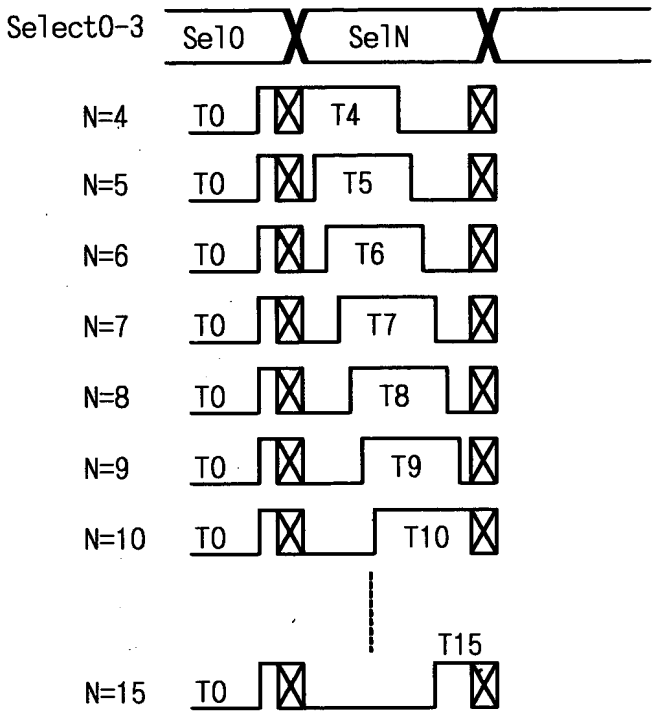

Select0-3
Sel0
SelN
N=4
T0
T4
N=5
T0
T5
N=6
T0
T6
N=7
T0
T7
N=8
T0
T8
N=9
T0
T9
N=10
T0
T10
T15
N=15
T0

FIG. 4

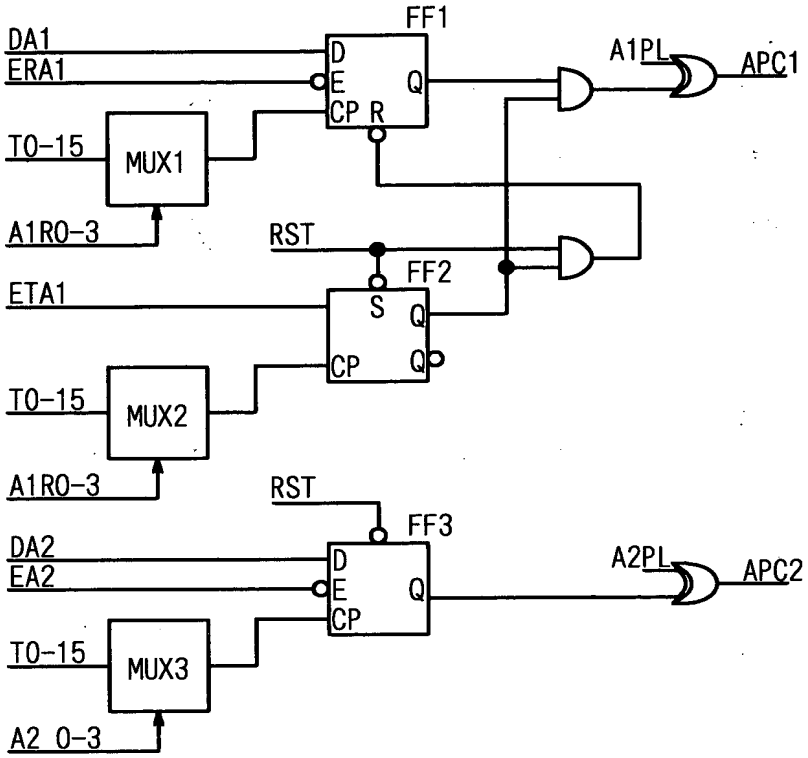

FF1
DA1
ERA1
D
E
CP
R
Q
A1PL
APC1
T0-15
MUX1
A1R0-3
RST
FF2
ETA1
S
Q
CP
Q
T0-15
MUX2
A1R0-3
RST
FF3
DA2
EA2
D
E
CP
Q
A2PL
APC2
T0-15
MUX3
A2 0-3

FIG. 5

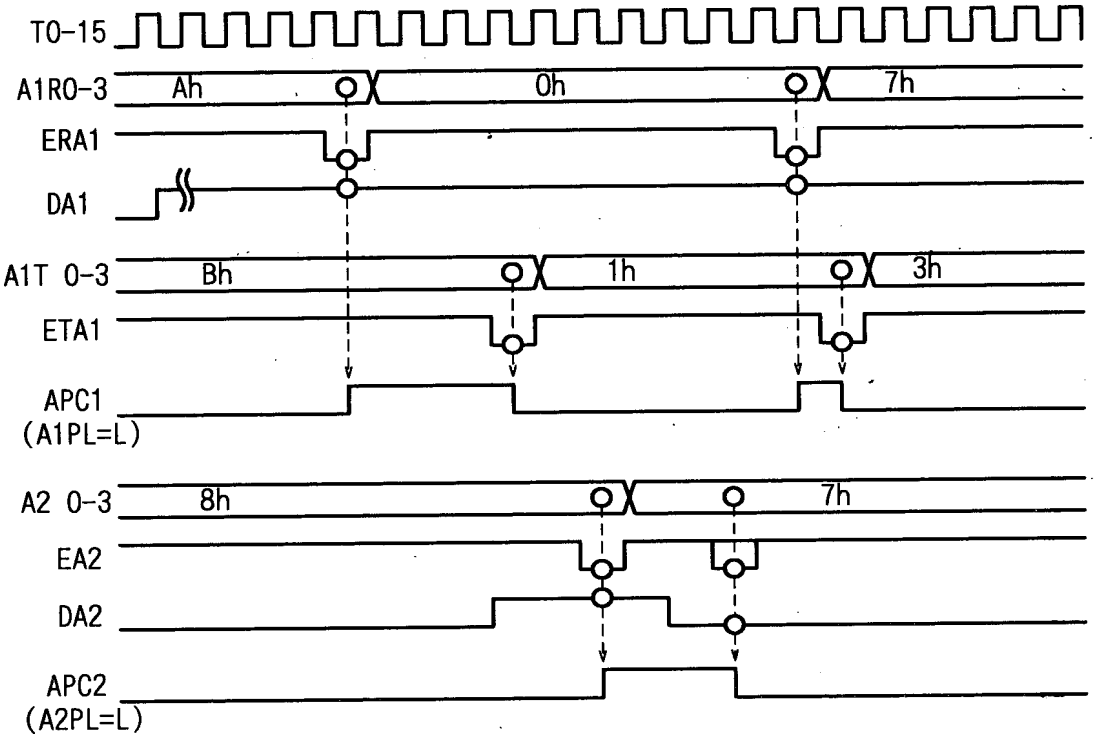

T0-15
A1R0-3
Ah
0h
7h
ERA1
DA1
A1T 0-3
Bh
1h
3h
ETA1
APC1
(A1PL=L)
A2 0-3
8h
7h
EA2
DA2
APC2
(A2PL=L)

FIG. 6

signals	contents	Active
RST	reset	L
TO-15	Fine Clock input	
DA1	APC1 Leading data	
ERA1	APC1 Leading Enable	L
A1RO-3	APC1 Leading Clk Select	
ETA1	APC1 Training Enable	L
A1TO-3	APC1 Training Clk Select	
DA2	APC2 data	
EA2	APC2 Enable	L
A2 0-3	APC2 Clk Select	

signals	contetns	Active
RST	reset	L
TO-15	Fine Clock input	
DA1	APC1 Leading data	
ERA1	APC1 Leading Enable	L
A1RO-3	APC1 Leading Clk Select	
ETA1	APC1 Training Enable	L
A1TO-3	APC1 Training Clk Select	
DA2	APC2 data	
EA2	APC2 Enable	L
A2 0-3	APC2 Clk Select	

FIG. 7

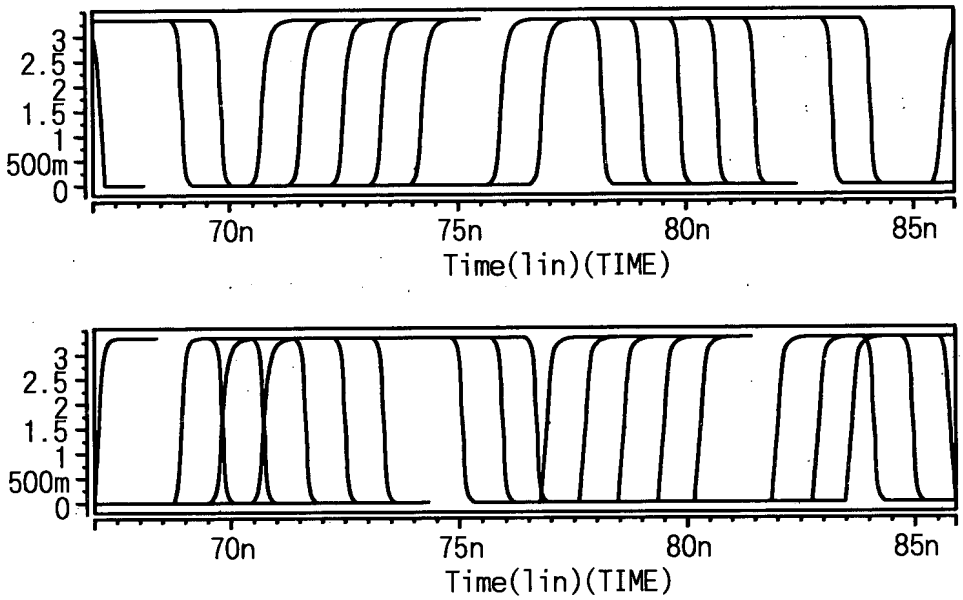

3
2.5
2
1.5
1
500m
0
70n
75n
80n
85n
Time(lin)(TIME)
3
2.5
2
1.5
1
500m
0
70n
75n
80n
85n
Time(lin)(TIME)

FIG. 8

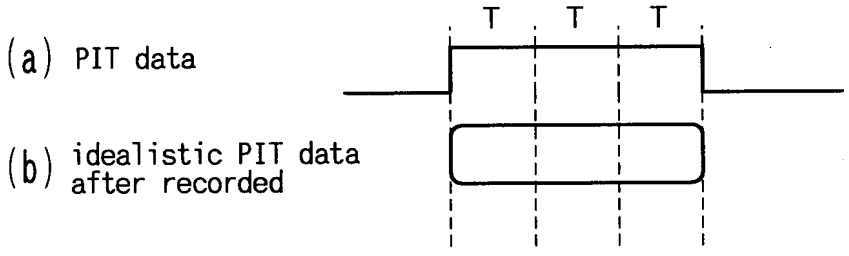

(a) PIT data
(b) idealistic PIT data after recorded
T
T
T

FIG. 9

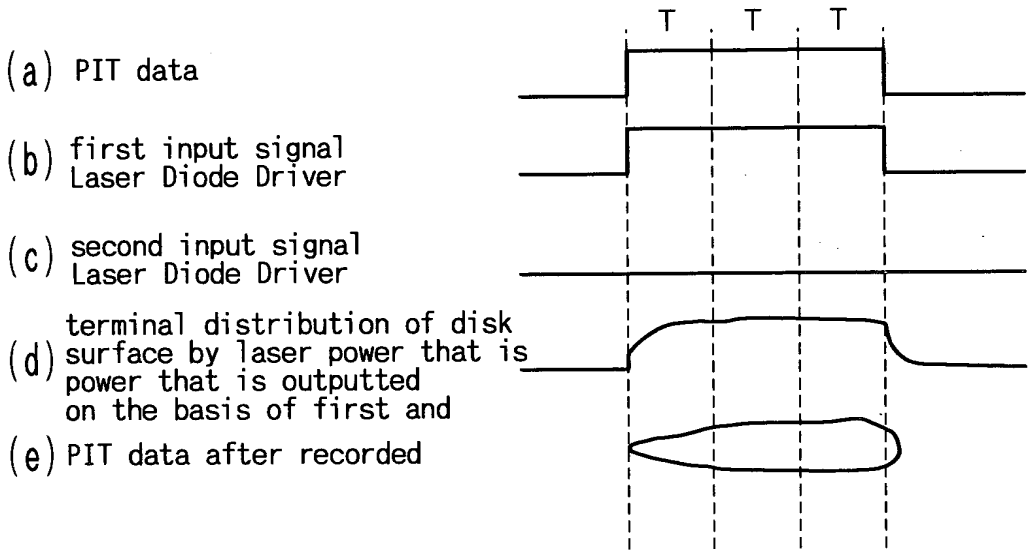

T
T
T
(a) PIT data
(b) first input signal Laser Diode Driver
(c) second input signal Laser Diode Driver
(d) terminal distribution of disk surface by laser power that is power that is outputted on the basis of first and
(e) PIT data after recorded

FIG. 10

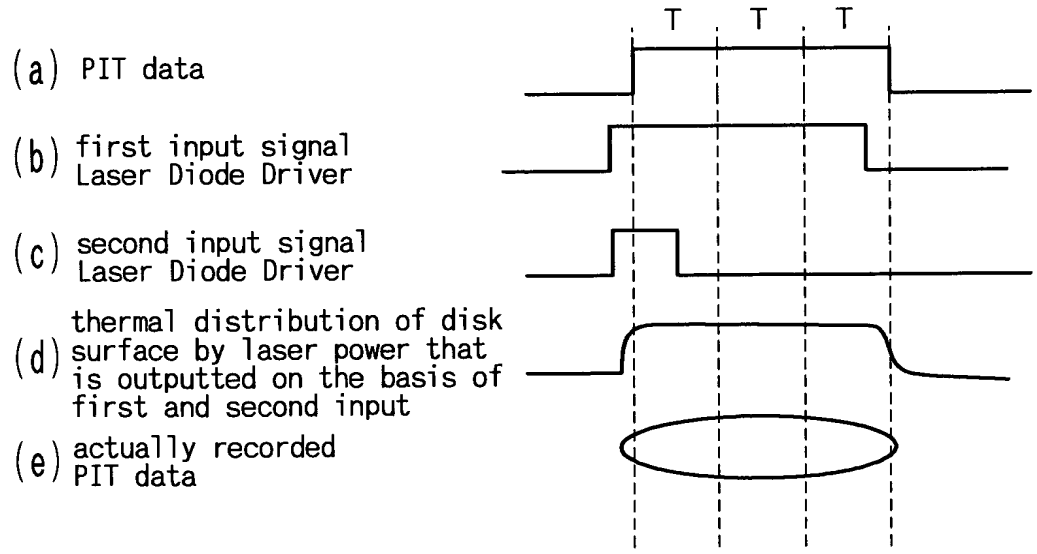

T
T
T
(a) PIT data
(b) first input signal Laser Diode Driver
(c) second input signal Laser Diode Driver
(d) thermal distribution of disk surface by laser power that is outputted on the basis of first and second input
(e) actually recorded PIT data

FIG. 11

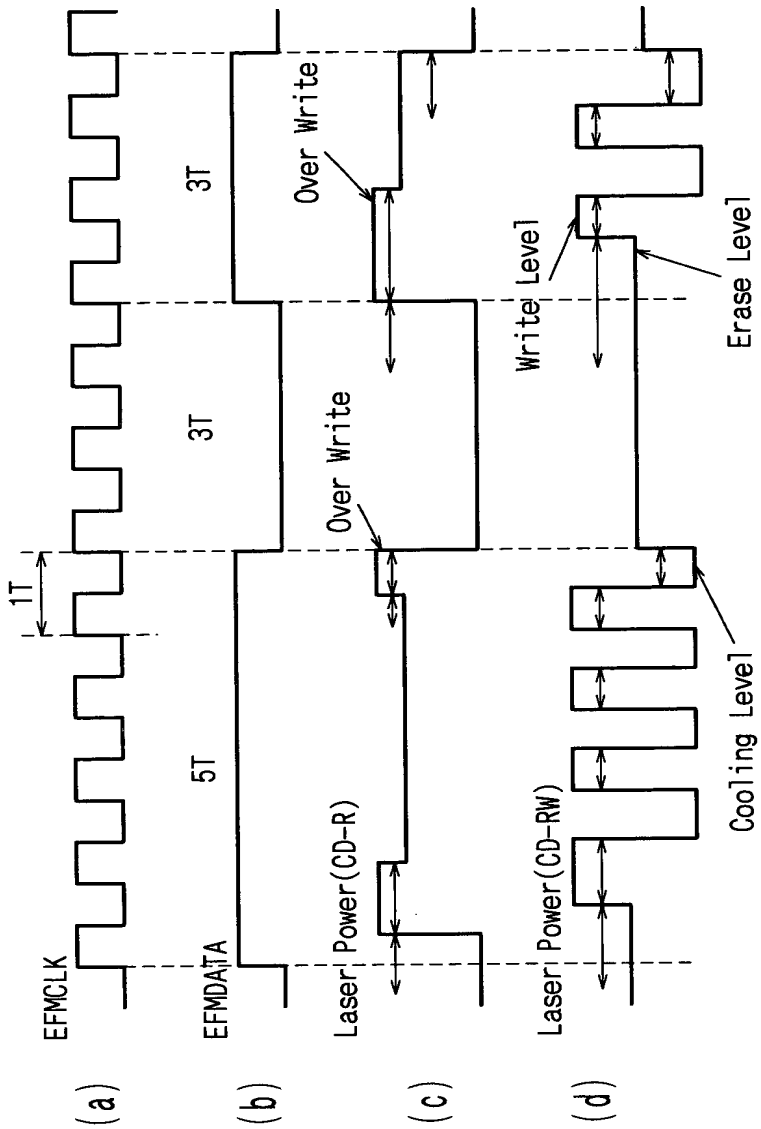

(a)
(b)
(c)
(d)
EFMCLK
EFMDATA
1T
3T
3T
5T
Over Write
Over Write
Laser Power(CD-R)
Laser Power(CD-RW)
Write Level
Erase Level
Cooling Level

FIG. 12

recording speed	EFMCLK [MHz]	T(period) [ns]	T/16 [ns]
1	4.32	231.38	14.46
2	8.64	115.69	7.23
4	17.28	57.85	3.62
8	34.57	28.92	1.81
16	69.14	14.46	0.90
32	138.29	7.23	0.45
36	155.58	6.42	0.40
40	172.87	5.78	0.36
48	207.44	4.82	0.30

FIG. 13

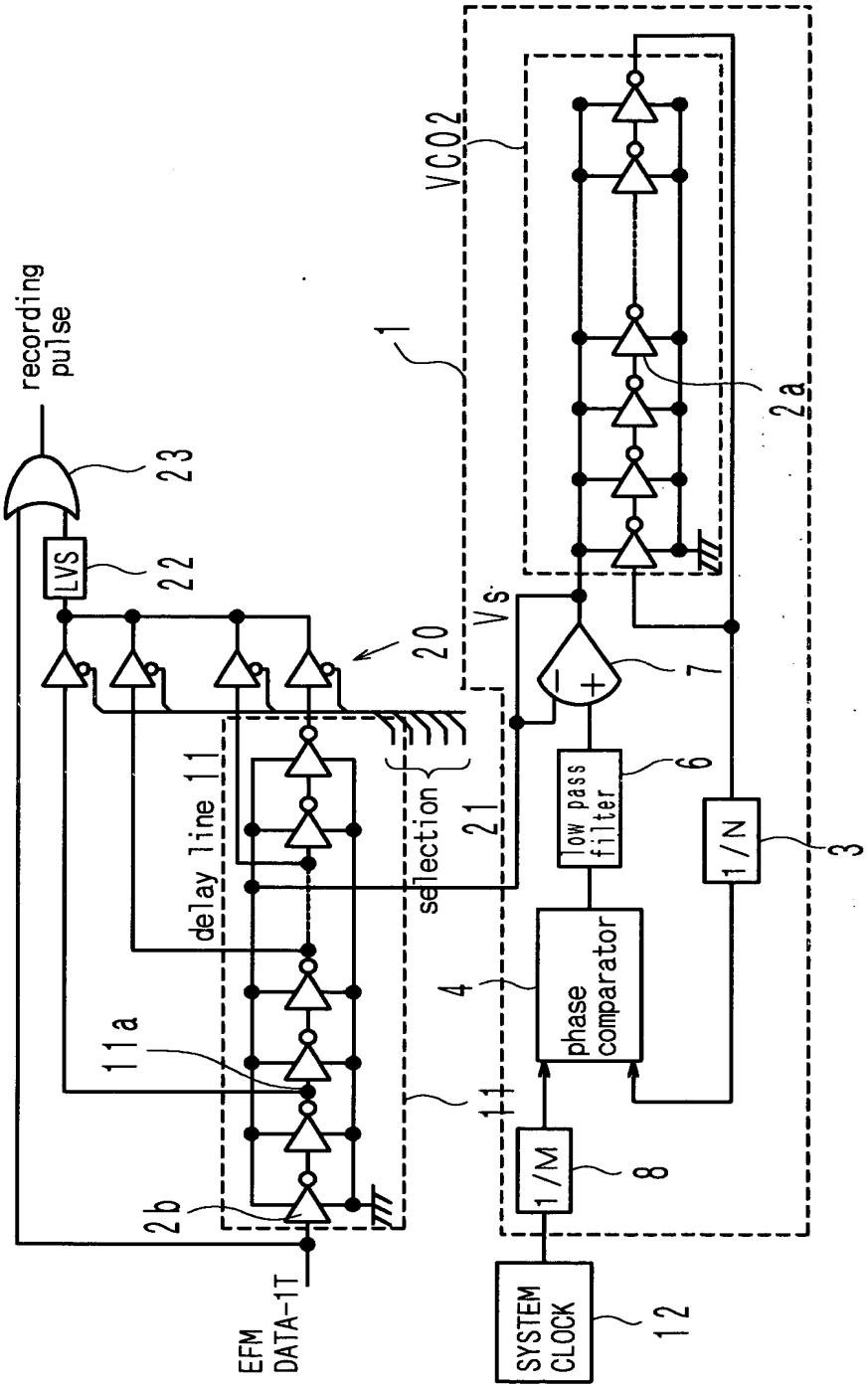
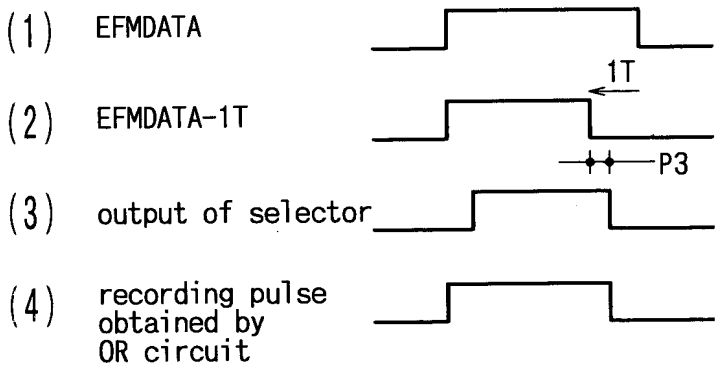

recording pulse
23
LVS
22
20
delay line 11
selection
21
11a
2b
EFM DATA-1T
VCO2
1
2a
Vs
7
low pass filter
6
1/N
3
4
phase comparator
11
1/M
8
SYSTEM CLOCK
12

FIG. 14


(1) EFMDATA
1T
(2) EFMDATA-1T
P3
(3) output of selector
(4) recording pulse obtained by OR circuit